6-1-2 I/O Memory Area Structure

Area		Size	Range	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status	Reference
							Read	Write				
CIO Area	I/O Area	2,560 bits (160 words)	CIO 0 to CIO 159*1	Basic I/O Units	OK	OK	OK	OK	OK	Cleared*2	OK	6-8
	Data Link Area	3,200 bits (200 words)	CIO 1000 to CIO 1199	Data links or PLC links (conditional)	OK	OK	OK	OK	OK		OK	6-13
	Synchronous Data Refresh Area	1,536 bits (96 words)	CIO 1200 to CIO 1295	Synchronous Units*3	OK	OK	OK	OK	OK		OK	6-14
	CPU Bus Unit Area	6,400 bits (400 words)	CIO 1500 to CIO 1899	CPU Bus Units (conditional)	OK	OK	OK	OK	OK		OK	6-15
	Special I/O Unit Area	15,360 bits (960 words)	CIO 2000 to CIO 2959	Special I/O Units (conditional)	OK	OK	OK	OK	OK		OK	6-16
	Serial PLC Link Area	1,440 bits (90 words)	CIO 3100 to CIO 3189	Linked PLC	OK	OK	OK	OK	OK		OK	6-17
	DeviceNet Area	9,600 bits (600 words)	CIO 3200 to CIO 3799	DeviceNet Master (fixed allocations) (conditional)	OK	OK	OK	OK	OK		OK	6-18
	Internal I/O Area	3,200 bits (200 words) 37,504 bits (2,344 words)	CIO 1300 to CIO 1499 CIO 3800 to CIO 6143	---	OK	OK	OK	OK	OK		OK	---
Work Area		8,192 bits (512 words)	W000 to W511	---	OK	OK	OK	OK	OK	Cleared *2	OK	6-19
Holding Area*4		8,192 bits (512 words)	H000 to H511	---	OK	OK	OK	OK	OK	Maintained	OK	6-20
Auxiliary Area		48,128 bits (3,008 words)	A000 to A447	---	OK	OK	OK	No	No	Depends on the address	No	6-22
			A448 to A959	---	OK	OK	OK	OK	OK			
			A960 to A1471*5	---	OK	OK	OK	OK	OK			
			A10000 to A11535*5	---	OK	OK	OK	No	No			

*1 The I/O Area can be expanded to include CIO 0160 to CIO 0999 by changing the first words allocated to specified Units. Settings for the first words can be made using the CX-Programmer to set the first words in the I/O tables. The setting range for the first words is CIO 0 to CIO 900.

*2 If the I/O Memory Hold Flag (A500.12) is ON, the memory values will be maintained when the operating mode is changed. If, in addition, the PLC Setup is set to hold the status of the I/O Memory Hold Flag at startup (IOM Hold Bit parameter), the memory values will be maintained when the power supply is turned ON.

*3 This area is supported only by CJ2H CPU Units. “Synchronous Units” are CPU Bus Units and Special I/O Units that support synchronous unit operation.

*4 H512 to H1535 can be set for use only as function block memory or SFC memory.

*5 A960 to A1471 and A10000 to A11535 were added to expand the Auxiliary Area in CJ2 CPU Units. These words cannot be accessed by CPU Bus Units, Special I/O Units, PTs, and Support Software that do not specifically support the CJ2 CPU Units.
Only the following CPU Bus Units and Special I/O Units specifically support the CJ2 CPU Units.

- EtherNet/IP Unit: CJ1W-EIP21
- Position Control Units: CJ1W-NC214, CJ1W-NC234, CJ1W-NC281, CJ1W-NC414, CJ1W-NC434, CJ1W-NC481, and CJ1W-NC881
- Analog Input Unit: CJ1W-AD042
- Analog Output Unit: CJ1W-DA042V
- Serial Communications Units: CJ1W-SCU22, CJ1W-SCU32, and CJ1W-SCU42

Area	Size	Range	External I/O allocation	Bit access	Word access	Access		Change from Programming Device	Status at startup or mode change	Forcing bit status	Reference
						Read	Write				
TR Area	16 bits	TR0 to TR15	---	OK	---	OK	OK	No	Cleared	No	6-23
DM Area	32,768 words	D00000 to D32767	---	OK*7	OK	OK	OK	OK	Maintained	No	6-24
EM Area	32,768 words per bank, 25 banks max. (0 to 18 hex)	E00_0 to E18_32767*7	---	OK*7	OK	OK	OK	OK	Maintained	Can be enabled with a setting.*8	6-27
Timer Completion Flags	4,096 bits	T0 to T4095	---	OK	---	OK	OK	OK	Cleared	OK	6-31
Counter Completion Flags	4,096 bits	C0 to C4095	---	OK	---	OK	OK	OK	Maintained	OK	6-33
Timer PVs	4,096 words	T0 to T4095	---	---	OK	OK	OK	OK	Cleared	No*9	6-31
Counter PVs	4,096 words	C0 to C4095	---	---	OK	OK	OK	OK	Maintained	No*10	6-33
Task Flag Area	128 bits	TK000 to TK127	---	OK	---	OK	No	No	Cleared	No	6-34
Index Registers*6	16 registers	IR0 to IR15	---	OK	OK	Indirect addressing only	Specific instructions only	No	Cleared	No	6-35
Data Registers*6	16 registers	DR0 to DR15	---	No	OK	OK	OK	No	Cleared	No	6-40
Condition Flags	Example: Always ON Flag	System symbols in the global symbols table of the CX-Programmer (e.g., P_On)	---	OK	---	OK	No	No	Cleared	No	6-42
Pulse bits	Example: 1 s Clock Pulse	System symbols in the global symbols table of the CX-Programmer (e.g., P_1s)	---	OK	---	OK	No	No	Cleared	No	6-44

*6 Index registers and data registers can be used either individually by task or they can be shared by all the tasks.

*7 Banks D to 18 hex of the EM Area were added to expand the EM Area in CJ2 CPU Units. Also, the ability to address bits in the DM Area and EM Area was also added as a new feature to the CJ2 CPU Units.
Banks D to 18 hex of the EM Area cannot be accessed and bit addresses in the DM Area and EM Area cannot be used by CPU Bus Units, Special I/O Units, PTs, and Support Software that do not specifically support the CJ2 CPU Units.
Only the following CPU Bus Units and Special I/O Units specifically support the CJ2 CPU Units.

- EtherNet/IP Unit: CJ1W-EIP21
- Position Control Units: CJ1W-NC214, CJ1W-NC234, CJ1W-/NC281, CJ1W-NC414, CJ1W-NC434, CJ1W-NC481, and CJ1W-NC881
- Analog Input Unit: CJ1W-AD042
- Analog Output Unit: CJ1W-DA042V
- Serial Communications Units: CJ1W-SCU22, CJ1W-SCU32, and CJ1W-SCU42

*8 Bits in the specified bank and all banks after it can be force-set/reset. (This is called the EM Area force-set/reset function.) With CJ2H CPU Units, bits in following EM Area banks that are set for automatic address allocation can be force-set/reset.
CJ2H-CPU64/65(-EIP): E03_0 to E03_32767
CJ2H-CPU65(-EIP): E06_0 to E09_32767
CJ2H-CPU67(-EIP): E07_0 to E0E_32767
CJ2H-CPU68(-EIP): E11_0 to E18_32767

*9 Timer PVs can be refreshed indirectly by force-setting/resetting Timer Completion Flags.

*10 Counter PVs can be refreshed indirectly by force-setting/resetting Counter Completion Flags.